Abstract

[0076] A pre-stored vector interrupt handling system for rapidly processing interrupt requests from input/output (I/O) devices in processor-based systems includes selection logic and an interrupt vector store to quickly deliver a branch instruction from the interrupt vector store directly to the execution unit of a processor. The interrupt vector store is either pre-loaded with a table of the processor's branch instructions during system initialization or implemented in ROM. During normal operation, when an interrupt is received, a master interrupt signal is issued to the processor, which asserts an instruction cycle mode signal to external chip select logic. The chip select logic de-selects the program store and selects the interrupt vector store. An interrupt vector from the vector store is loaded onto the data bus and then directly into the execution unit of the processor.